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(54) Image sensor array.

(57) A linear image sensor array with a row (16) of photodiodes (14) and a transfer circuit (20) for each photodiode (14), the circuit having a pair of transistors for two stage transfer of the image signal charge from the photodiode to the gate of one transistor of a two transistor source follower (30, 32; 33), a transistor (36) for applying a bias charge to the photodiode, a multiplexing transistor (34) for connecting the source follower output to an output line (22), a reset transistor (38) for resetting the source follower, and clock signals for operating the transfer circuits in succession to serially output image signals to the output line.

FIG. 2

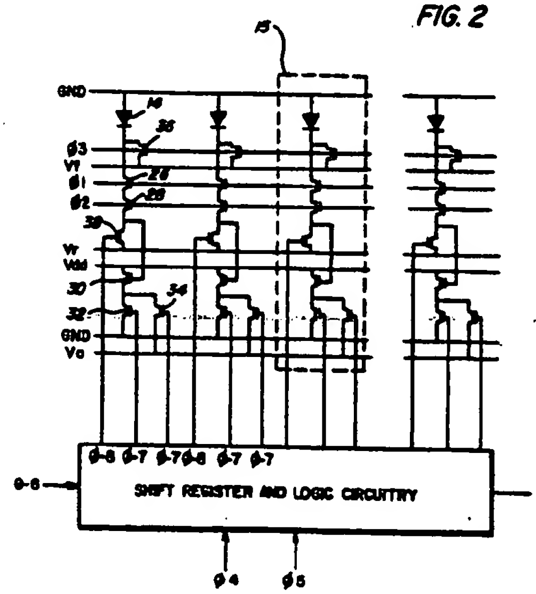

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IMAGE SENSOR ARRAY

The invention relates to an image sensor array having at least one array of photodiodes, and means associated with each photodiode for amplifying and transferring the image signal charge of each photodiode to an output line.

In order to achieve high resolution imaging, an image sensor array having a relatively large number of photosites is required. However, attempts to provide an array with a high number of photosites have been generally unsuccessful and yields are low. An alternate arrangement envisions taking several image sensor arrays and butting them together in end to end relation to form a longer composite array. Indeed, if this technology can be successfully practiced, full width or contact scanning arrays can be formed equal in size to the largest image to be scanned.

In considering the merits of joining sensor arrays together, it is deemed highly advantageous that pitch across the entire array be maintained and for this reason, it is important that spacing between adjoining photosites at the butted ends of the individual arrays be the same as the spacing between the photosites in the body of the arrays. In fabricating image sensor arrays, and especially image sensor arrays having the attributes necessary for end to end abutting with other like arrays, it is desirable to use NMOS or CMOS technology in order to take advantage of the very high yields possible with these types of technology. However, using NMOS or CMOS technology, single stage charge transfer can result in poor transfer efficiency between the high capacitance of the array photosites and the low input capacitance of the output charge to voltage converters.

The invention seeks to provide an improved image sensor array having high transfer efficiency, in which there is provided: a source follower with each sensor photosite for charge to voltage conversion of the image signal charge of the sensor photosites; two stage transfer means for transferring the image signal charge efficiently from the sensor photosites to the source follower and for minimizing feedback; means with each source follower for injecting a bias charge into the sensor photosites for transmittal to the source follower to enhance transfer efficiency; and switching means for outputting the image signal voltage from the source follower to the output.

IN THE DRAWINGS:

Figure 1 is a schematic view of an image scanning array having an array of photosites in the form of photodiodes incorporating the two stage transfer of the present invention;

Figure 2 is a circuit schematic showing details of the transfer circuit associated with each photodiode in the array for effecting two stage transfer of the image signals from the photodiodes to an output line;

Figure 3 is a detailed circuit schematic of the transfer circuit;

Figure 4 is a timing diagram showing the operating clock signal waveform for the image scanning array with two stage transfer shown in Figure 1; and

Figure 5 is a timing diagram depicting a modified operating clock signal waveform for resetting the transfer circuits of the array photodiodes in unison.

Referring to Figure 1, there is shown the image sensor array with two stage transfer, designated generally by the numeral 10, of the present invention. Image sensor array 10 includes a base or chip 12 of silicon with a plurality of photosites in the form of photodiodes 14 thereon. Photodiodes 14 are in closely spaced juxtaposition with one another on chip 12 in a linear array or row 16. Several smaller arrays such as array 10 can be abutted together end to end with one another to form a longer array, i.e. a full width or contact array, with spacing between the photodiodes at the butted ends the same as the spacing between the photodiodes inside the chip thereby maintaining photodiode pitch across the entire full width of the composite array.

While photodiodes 14 are shown and described herein, other photosite types such as amorphous silicon or transparent electrode MOS type photosites may be envisioned. Further, while a one dimensional sensor array having a single row 16 of photodiodes 14 is shown and described herein, a two dimensional sensor array with plural rows of photodiodes may be contemplated.

Each photodiode 14 has a two stage transfer circuit 20 associated therewith which together with the photodiode form a pixel cell 15. In circuit 20, the image charge signal from the photodiode is transferred to the input of a source follower 33 (shown in Figures 2 and 3), which feeds the signal to an output line 22 as a voltage. In addition, the image signal charge is amplified due to the gain achieved during transfer of the image signal charge from photodiode 14 to the input of source follower

33. The signal gain results from the difference in capacitance between photodiode 14 and the input of the source follower 33. This brings the image charge signal to a desired potential level prior to transferring the charge to line 22. Suitable shift register and logic circuitry 24 provides timing control signals for connecting each pixel cell 15 to line 22 in the proper timed sequence.

Image sensor array 10 may for example be used to raster scan a document original, and in that application, the document original and the sensor array 10 are moved or stepped relative to one another in a direction that is normally perpendicular to the linear axis of array 10. At the same time, the image line being scanned is illuminated and suitable optical means such as a gradient index fiber lens array provided to focus the photodiodes 14 on the image line. During an integration period, a charge is developed on each photodiode. This charge is proportional to the reflectance of the image area viewed by each photodiode. The image signal charges are thereafter transferred by the circuits 20 to output line 22 in a predetermined step by step timed sequence as will appear.

Referring particularly to Figures 2 and 3, each transfer circuit 20 includes a source follower or common drain amplifier 33 composed of transistors 30, 32 for converting the image signal charge to a voltage signal. Two stage transfer, consisting of transistors 26, 28 in series with the line 25 connecting one electrode of photodiode 14 with the gate of transistor 30 of source follower 33, is utilized for transferring the image signal charge from the photodiode 14 to source follower 33 to minimize feedback due to the transistor dynamic drain conductance effect. The other electrode of photodiode 14 and the source of transistor 32 are grounded through ground line 29.

The drain of transistor 30 is connected to a preset voltage potential V-dd by line 40. The source of transistor 30 and the drain of transistor 32 of source follower 33 are connected by line 44 to multiplexing transistor 34 which connects the pixel cell to output line 22. A charge injection transistor 36 is provided to inject a preset bias charge, for example, an electrical fat zero V-fz, into photodiode 14. A reset transistor 38 controls application of a reset signal from a predetermined reset signal source Vr to the gate of transistor 30 of source follower 33.

A suitable pixel clock (not shown) provides clock signals ϕ_1, ϕ_2 and ϕ_3 controlling lateral transfer of the image signal charge from photodiodes 14 to source followers 33. Additional clock signals ϕ_4 and ϕ_5, and shift register clock signal ϕ_6 are input to shift register and logic circuitry 24. Shift register and logic circuitry 24, which includes one or more shift registers, outputs clock signals ϕ_7 and ϕ_8 for operating transfer circuits 24 to amplify and transfer the image signal voltage from source followers 33 to output line 22 serially. As will be understood, clock signals ϕ_1 through ϕ_8 synchronize and integrate operation of scanning array 10 with other component parts of the scanning system with which array 10 is associated, and with additional arrays in the event array 10 is abutted with other like arrays to form a longer scanning array.

In operation and referring particularly to Figures 2 and 4, following the integration period, a lateral charge transfer cycle for all photodiodes 14 is initiated in which clock signals ϕ_1, ϕ_2 actuate the two stage transfer transistors 26, 28 of circuit 20 for all pixel cells 15 concurrently. Transistors 26, 28 transfer the image signal charge built up on the individual photodiodes 14 during the integration period to the gates of transistors 30 of source followers 33. Thereafter, clock signals ϕ_3 and Vfz actuates transistors 36 to place the bias voltage charge Vfz on the photodiodes 14.

Following the lateral charge transfer cycle, a video output cycle is commenced in which the clock signals ϕ_7 and ϕ_8 output by shift register and logic circuitry 24 are shifted successively along the row of transfer circuits of each pixel cell 15 to activate the source followers 33 and to serially connect the outputs of the source followers to output line 22. In each pixel cell, the clock signal ϕ_7 input to the gate of transistor 32 of source follower 33 and the gate of output transistor 38 actuates transistors 32, 38 to output the image signal voltage Vo to line 22. Following a predetermined interval, clock signal ϕ_8 triggers reset transistor 38 to apply reset signal Vr to the gate of transistor 30, resetting source follower 33 and terminating output of the signal voltage for that pixel cell.

The foregoing is repeated along the row of photodiodes 14 for each pixel cell 15 until the output corresponding to the last photodiode in the row 16 of photodiodes 14 has been transferred.

In the embodiment shown in Figure 5, where like numerals refer to like parts, clock signal ϕ_8 is used to trigger the reset transistors 38 of all transfer circuits 20 simultaneously. Triggering of reset transistors 38 simultaneously applies reset potential Vr to the gates of transistors 30, resetting the source followers 33 of transfer circuits 20 in unison.

While the invention has been described with reference to the structure disclosed, it is not confined to the details set forth, but is intended to cover such modifications or changes as may come within the scope of the following claims.

Claims

1. In an image sensor array having at least one array of photodiodes, and means associated with each photodiode for amplifying and transferring the image signal charge of each photodiode to an output line, comprising:

a) source follower means for charge to voltage conversion of the photodiode image signal charge to an image signal voltage;

b) two stage transfer means for transferring the image signal charge from the photodiode to the input of said source follower means, transfer of said signal charge by said two stage transfer means amplifying said signal charge while minimizing feedback;

c) means for injecting a bias charge on the photodiode;

d) switching means for coupling the output of said source follower means to said output line whereby the image signal charge from said photodiode following charge to voltage conversion by said source follower means is transferred to said output line; and

e) reset means for resetting said source follower means following output of said image signal voltage to said output line.

2. The image sensor array according to claim 1 in which said two stage transfer means comprises a switch pair in series between the photodiode and said source follower means input; and

clock means for actuating said switch pair in succession to transfer the image signal charge from the photodiode to said source follower means input.

3. The image sensor array according to claim 1 or claim 2 in which said injecting means includes a source of preset potential; and

a switch for coupling said potential to the photodiode whereby to apply said potential to the photodiode and inject said bias charge.

4. The image sensor array according to claim 3 including:

clock means for actuating said switch following transfer of the image signal charge from the photodiode to said source follower means input but before transfer of said image signal voltage to said output line by said switching means.

5. The image sensor array according to any preceding claim in which said reset means includes:

a reset signal source; and

a reset switch for coupling said reset signal source to said source follower means input.

6. The image sensor array according to claim 5 including:

clock means for triggering said reset switch following output of said image signal voltage by said switching means.

7. The image sensor array according to claim 5 including:

clock means for triggering each of said reset switches simultaneously whereby to reset the source followers associated with each of said photodiodes in unison.

8. The image sensor array according to claim 1 including clock means for actuating said two stage transfer means for each of said photodiodes in unison to transfer the image signal charges from the photodiode to the input of the source follower means associated therewith and then actuating said injecting means for each of said photodiodes in unison to inject said bias charge on said array of photodiodes in unison,

said clock means thereafter actuating said switching means for each of said source follower means individually in succession to serially transfer the image signal voltage from said source follower means to said output line.

9. In an image sensor array having at least one array of photodiodes, and means associated with each photodiode for transferring the image signal charge of each photodiode to an output line, comprising:

a) a source follower for charge to voltage conversion of the image signal charge to an image signal voltage;

b) a switch pair in series between the photodiode and one input of said source follower for transferring the image signal charge from the photodiode to said source follower, transfer of said signal charge by said switch pair amplifying said signal charge while minimizing feedback;

c) a first switch for injecting a bias charge on the photodiode for transmittal to a second input of said source follower;

d) a second switch for coupling the output of said source follower to said output line;

e) clock means for actuating the switch pair and said first switches of all said photodiodes in unison to first transfer said image signal charge from the photodiode to said source follower and then inject said bias charge on said array of photodiodes,

said clock means thereafter actuating said second switch for each of said photodiodes in said photodiode array individually in succession to serially transfer the image signal voltage from said source followers to said output line.

FIG. 1

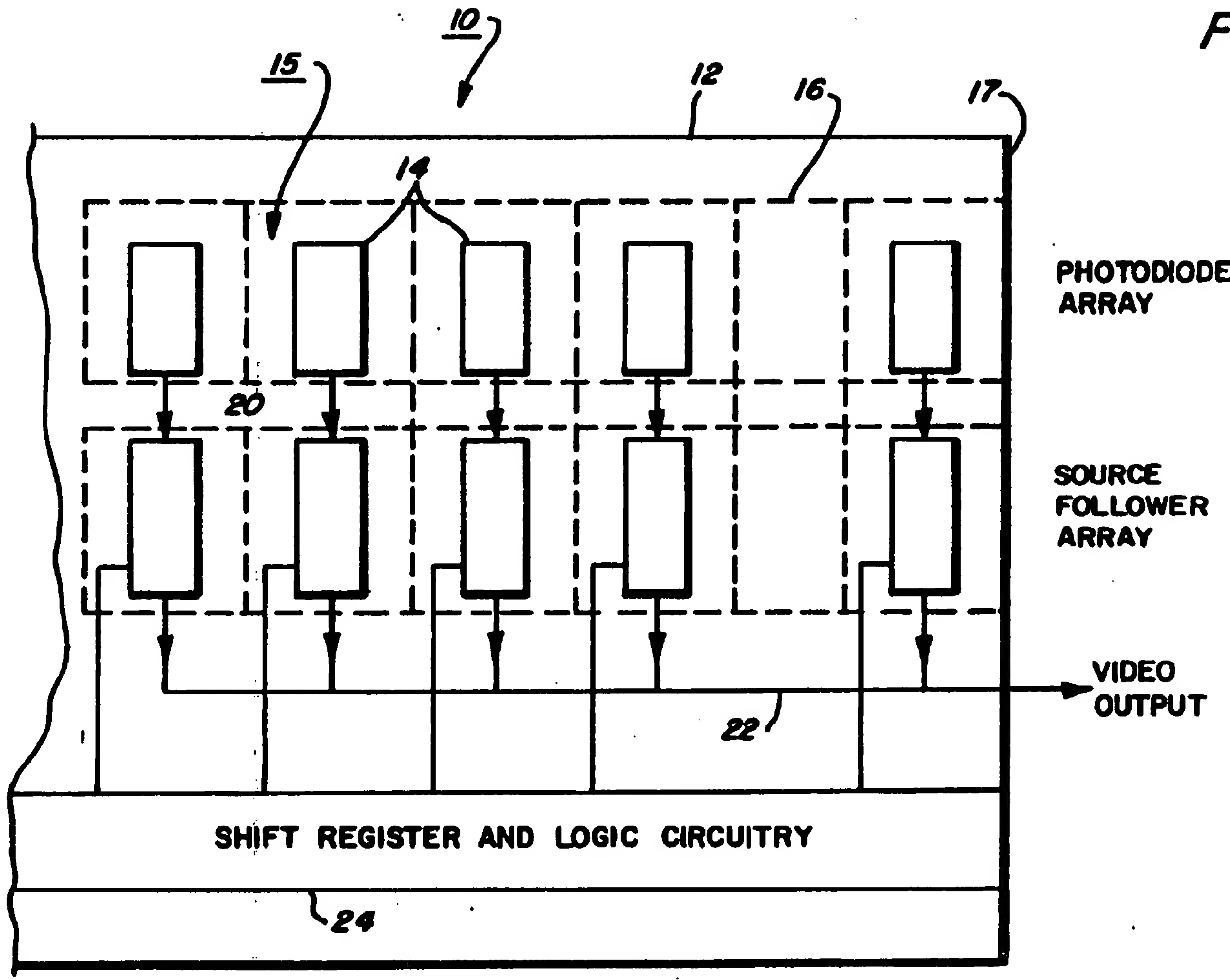
10
15
12
16
17
14
PHOTODIODE ARRAY
20
SOURCE FOLLOWER ARRAY
VIDEO OUTPUT
22
SHIFT REGISTER AND LOGIC CIRCUITRY
24

FIG. 2

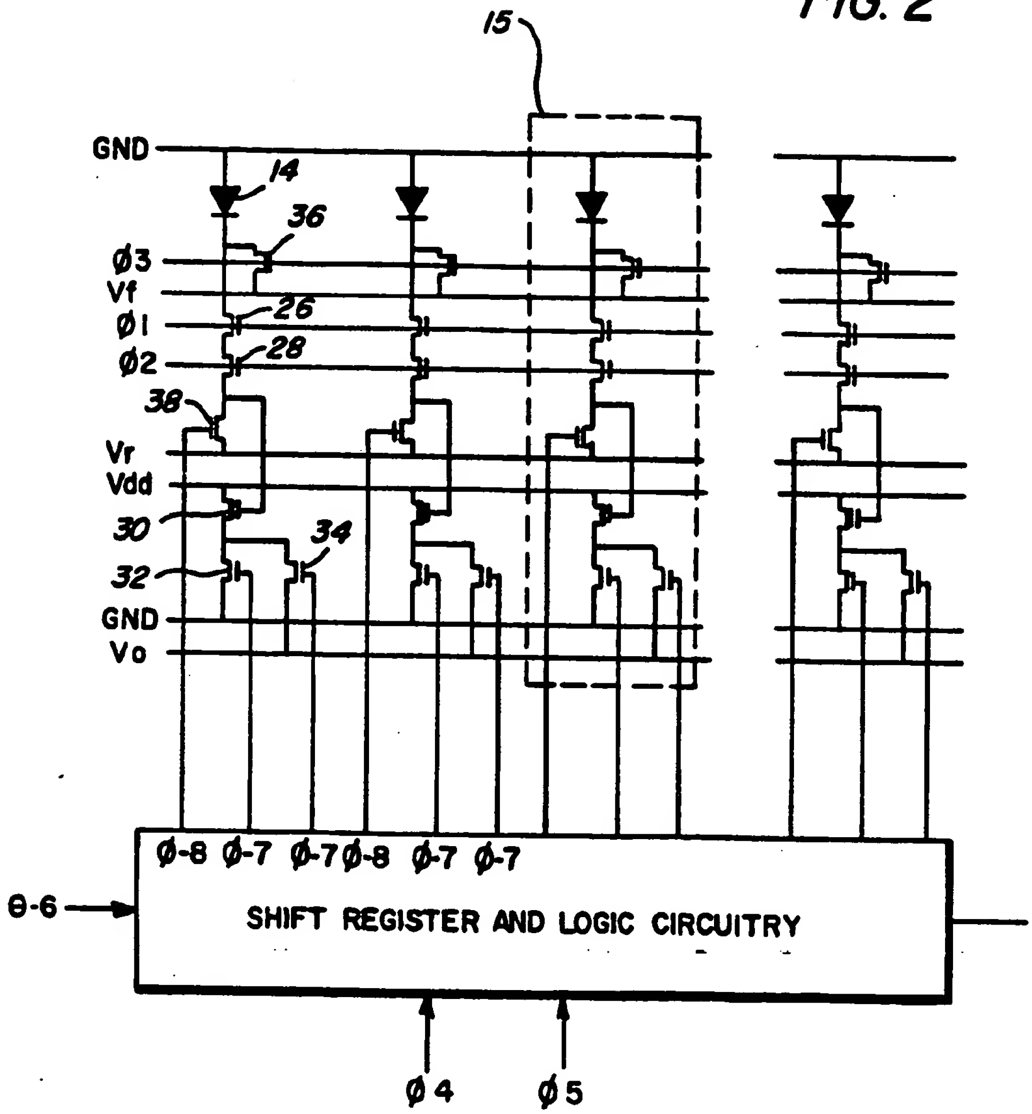
15
GND
14
36
Ø3
Vf
26
Ø1
28
Ø2
38
Vr
Vdd
30
34
32
GND
Vo
Ø-8 Ø-7 Ø-7 Ø-8 Ø-7 Ø-7
θ-6
SHIFT REGISTER AND LOGIC CIRCUITRY
Ø4
Ø5

FIG. 3

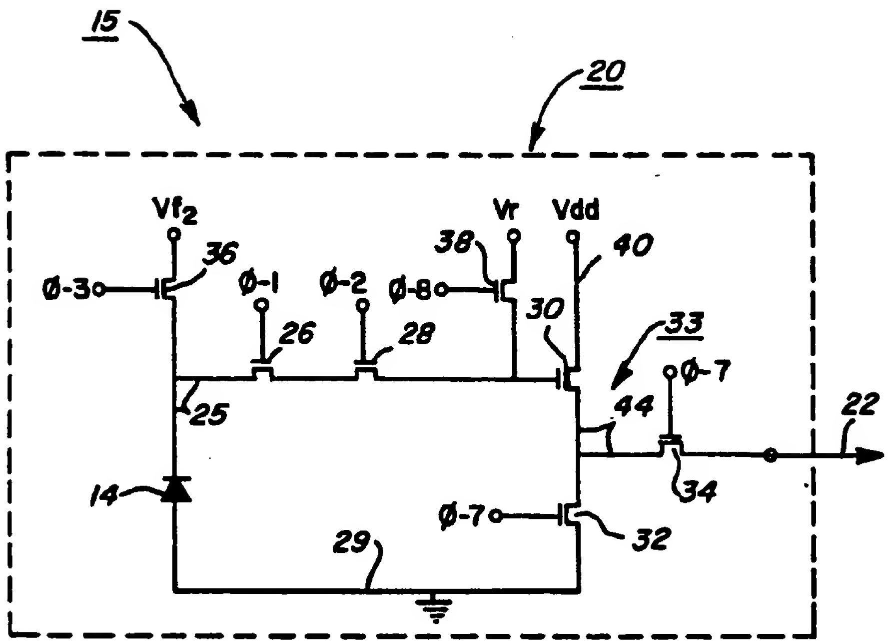
15
20
Vf2
Vr
Vdd
Ø-3
36
Ø-1
Ø-2
Ø-8
38
40
30
26
28
33
Ø-7
44
22
25
14
34
Ø-7
32
29

FIG. 4

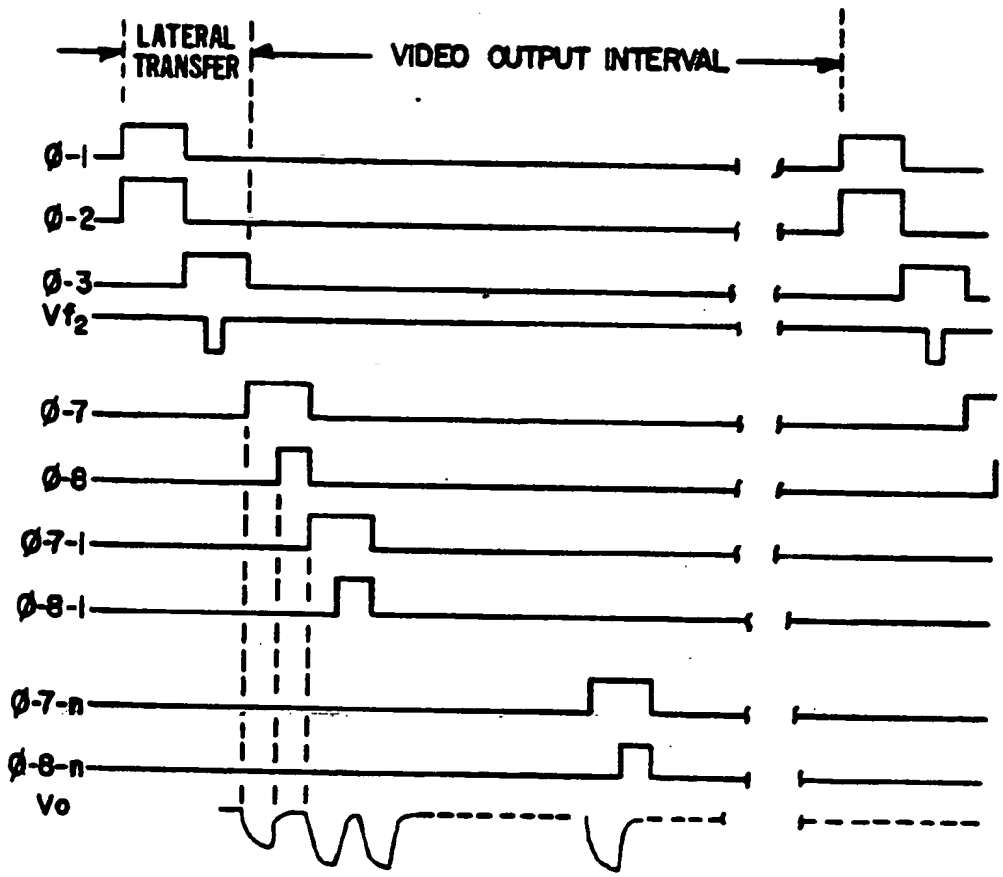
LATERAL TRANSFER
VIDEO OUTPUT INTERVAL
Ø-1
Ø-2
Ø-3
Vf2
Ø-7
Ø-8
Ø-7-1
Ø-8-1
Ø-7-n
Ø-8-n
Vo

FIG. 5